Summer 2017 Seminar Series

Power-Efficient and Reliable Network-on-Chips for Scalable Multicore Architectures

FRIDAY JUNE 2, 2017

11:00 AM – HEC 450

Today's microprocessor designers have resorted to exploiting parallelism by increasing the number of cores per die as a power-efficient approach to performance improvement the multicore era. Processor chips with tens to hundreds of cores are already in the market today, and projections call for thousands of cores on a chip within a decade in order to satisfy the nation's needs for high-performance computing.

The proliferation of multiple cores on the same die heralded the advent of communication-centric rather than computation-centric systems, to the forefront of computing design wherein the design of the Network-on-Chip (NoC) connecting various modules, namely the processing cores, cache banks, memory units and I/O devices, has become extremely important. As the number of cores on the chip keeps growing to satisfy power and performance scaling, the NoC design has become the most critical element to achieving the performance potential of future processor chips. Among the challenges facing current NoC design, power dissipation and reliability have been identified as the most critical ones.

In this talk, I will first discuss several research challenges facing multicore architectures and NoC design. Next I will present some of our ongoing efforts to address these issues using architectural innovations as well as a synergistic mix of emerging interconnect technologies. The talk will conclude with pointers to some future research directions in this area ed

Ahmed Louri

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Professor Louri was a member of the faculty of the University of Arizona's Department of Electrical and Computer Engineering from 1988 to 2015. At the University of Arizona, he also was the chair of the computer engineering program from 2000 to 2006 and the director of the High Performance Computing Architectures and Technologies Laboratory. From 2010 to 2013, he served as a program director in the Directorate for Computer and Information Science and Engineering (CISE) of the National Science Foundation.

Professor Louri is the recipient of the National Science Foundation Research Initiation Award (1989), the Best article Award from IEEE Micro, the Advanced Telecommunications Organization of Japan Fellowship, the Centre Nationale de Recherche Scientifique (CNRS), France, Fellowship, and the Japan Society for the Promotion of Science Fellowship, and several teaching awards. He was instrumental in bringing optical interconnects into mainstream research in interconnection networks and bridging the gap between computer architecture and optics research communities.

Professor Louri is a Fellow of IEEE, a regular member of OSA, a member of the International Society for Optical Engineering working Group on Optical Computing, a member of the IEEE Society Technical Committee on Computer Architecture, and a member of the IEEE Technical Committee on Parallel Processing.